VERIFICATION OF TRANSLATION

I, the undersigned, declare that I am fluent in the English and Korean language. I am competent to translate the attached document in Korean into English, and the above English translation of the document is accurate and complete.

Date: 28. July. 2005

Signature: [signature]

Typed Name: Yang Sukcheol

Address: _____

[Abstract of the Disclosure]

[Abstract]

The present invention is directed to a flash memory device for preventing program misjudgment of flash memory cells and has a uniform threshold voltage distribution and a program verify method of the same. The flash memory device includes a memory cell array block, a program verify voltage generating section for variably generating a program verify voltage to check whether flash memory cells are programmed, and a wordline level selecting section for transferring a program verify voltage to the flash memory cells. The program verify voltage generating section includes first to third resistors serially coupled between a power supply voltage and a ground voltage, a first NMOS transistor connected to both terminals of the first resistor to short-circuit the first resistor in response to a first program verify control signal, and a second NMOS transistor connected to both terminals of the second resistor to short-circuit the second resistor in response to a second program verify control signal. A program verify operation is performed using a program verify voltage level varying with selective activation of first and second program verify control signals, fully programming flash memory cells having an uncertainty whether they are programmed.

[Typical Figure]

FIG. 4

[Index]

program verify voltage, under program cell, threshold voltage

[Specification]

[Title of the Invention]

FLASH MEMORY DEVICE FOR VERIFYING SUCCESSFUL PROGRAMMING OF FLASH CELLS AND THE METHOD THEREOF

[Brief Description of the Drawings]

FIG. 1 shows a part of a conventional flash memory device.

FIG. 2 is a program verify timing diagram of the flash memory device shown in FIG. 1.

FIG. 3 shows distribution of threshold voltages Vt of a flash memory cells according to the program verify method of FIG. 2.

FIG. 4 shows a flash memory device according to an embodiment of the present invention.

FIG. 5 is a first exemplary program verify timing diagram adopting a program verify voltage according to the present invention.

FIG. 6 is distribution of threshold voltages of a flash memory cells according to the program verify method of FIG. 7.

FIG. 7 is a second exemplary program verify timing diagram adopting a program verify voltage according to the present invention.

FIG. 8 is a third exemplary program verify timing diagram adopting a program verify voltage according to the present invention.

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention relates to a semiconductor memory device and, more particularly, to a flash memory device for variably applying a program verify voltage.

Among non-volatile memory devices, flash memory devices are high-density data storage devices which are writable and erasable on boards. A flash memory cell is comprised of a field effect transistor (FET) including a select gate, a floating gate, a source, and a drain. Information is stored in a flash memory cell according to the change in the amount of charges on a floating gate when the amount of the charges varies with fluctuation of a threshold voltage Vt of a flash memory cell. Flash memory cell data is read out by applying a select voltage to a wordline connected to a select gate. A flash memory cell is passed by applying a select voltage, so that the amount of flowing current is determined by a threshold voltage Vt of a flash memory cell.

Generally, a flash memory cell exhibits two states, i.e., "programmed" and "erases" states. If a flash memory cell is programmed, few or no excessive electron exists on a floating gate. Thus, a lot of source-drain currents flow to the flash memory cell. A state of an erased flash memory cell is called logic "1".

FIG. 1 shows a part of a conventional flash memory device. Referring to this figure, a flash memory device 100 includes a memory cell array block 110, a row decoder 120, wordline level selecting sections 130, a driver section 140, a page buffer 150. The memory cell array block 110 includes i strings 200, 202, 204, and 206 to which flash memory cells are serially connected. Flash memory cells 112, 113, and 114 are serially connected to a first string 200. Gates of the flash memory cells 112, 113, and 114 are connected to first to sixteenth wordlines WLj (j=0, 1, ..., 15), respectively. A drain of the flash memory cell 11 connected to the first

wordline WL0 is connected to a first select transistor 111 whose gate is connected to a string select line SSL. A source of the flash memory cell 114 connected to a sixteenth wordline WL15 is connected to a second select transistor 115 whose gate is connected to a ground select line GSL. A drain of the first select transistor 112 is connected to a first bitline BL0, and a source of the second transistor 115 is connected to a common source line CSL.

The i strings 200, 202, 204, and 206 are connected to the string select line SSL, the first to sixteenth wordlines WLj (j=0, 1, ..., 15), and the ground select line GSL. Each of the strings 200, 202, 204, and 206 is connected to a page buffer 150 through bitlines BL0, BL1, ..., BLn-1, and BLi. The strings 200, 202, 204, and 206 constitute one page unit. For the convenience of description, FIG. 1 illustrates one page in the memory cell array block 110. However, a practical memory cell array block 110 includes a plurality of page units. The page units are addressed by the row decoder 120. In response to an addressing signal of the row decoder 120, transistors in the driver section 140 are turned on to select one page unit.

The wordline level selecting sections 130 select one voltage, among a program voltage VPGM, a read voltage VREAD, a program verify voltage VRDV, and a pass voltage VPASS, according to a corresponding mode and transfer the selected voltage to the driver section 140. The program voltage VPGM is applied during a program operation of selected flash memory cells, the read voltage VREAD is applied during a read operation thereof, and the program verify voltage VRDV is applied during verifying whether cells are programmed. The pass voltage VPASS passes unselected flash memory cells, allowing cell current to flow. The driver unit 140 applies a corresponding mode voltage to wordlines WLj (j=0, 1, ..., 15) in the selected on page unit in response to an addressing signal of the row decoder 120. The page buffer 150 senses cell current flowing through bitlines BL0, BL1,

..., BLi-1, and BLi to judge data of selected memory cells.

The flash memory device 100 iteratively performs one cycle for a program verify operation (hereinafter referred to as "program unit loop") after performing a program operation for flash memory cells. If the program verify operation is performed to determine that a flash memory cell is programmed, it is completed. If not, the program operation is performed again and a program verify read operation is iteratively performed. For example, assuming that the number of flash memory cells connected to one wordline WL is 4K, predetermined cycles are required for programming the flash memory cells and performing a program verify operation. If cycles are repeated to determine that flash memory cells connected to one wordline WL is completely programmed, another wordline WL is programmed and a program verify operation is iteratively performed.

If a program operation and a program verify operation are iteratively performed for one selected wordline WL, under-program flash memory cells are determined to be programmed and a program operation is completed. It is because while one program unit loop is iteratively performed, a program voltage VPGM rises and a program verify read voltage VRDV is regularly applied, as illustrated in FIG. 2. Due to unprogrammed flash memory cells, cell current increases during several program unit loops. This leads to level up of a command source line CSL. Here, if a regular program verify voltage VRDV is applied during a program unit loop performed subsequently, cell current decreases due to the level of the common source line CSL. Accordingly, misjudgement occurs that practically unprogrammed flash memory cells are programmed.

FIG. 3 is a diagram showing distribution of threshold voltages Vt of flash memory cells according to the program verify method of FIG. 2. Referring to this figure, threshold voltages Vt of all flash memory cells have negative voltage levels in an initial state where an erase operation is

performed for all flash memory cells. Thereafter, program unit loops are sequentially performed, so that as flash memory cells are programmed using a high program voltage, a threshold voltage Vt is distributed high and irregularly. Irregular distribution of flash memory cells having a high threshold voltage Vt results in over program that flash memory cells of a page unit are not erased completely during an erase operation.

Accordingly, there is a need for a flash memory device that prevents program misjudgement of flash memory cells and has a uniform threshold voltage distribution and a program verify method of the same.

[Technical Object of the Invention]

Therefore, it is an object of the invention to provide a flash memory device capable of preventing program misjudgement of flash memory cells.

It is another object of the invention to provide a program verify method capable of preventing program misjudgement of flash memory cells.

[Construction of the Invention]

In order to achieve the object, the present invention provides a flash memory device including a memory cell array block in which a plurality of flash memory cells are arranged; a program verify voltage generating section for variably generating a program verify voltage for checking whether the flash memory cells are programmed; and a wordline level selecting section for transferring the program verify voltage to a wordline connected to a control gate of the flash memory cells.

Preferably, the program verify voltage generating section includes a PMOS transistor and first to third resistors serially coupled between a power supply voltage and a ground voltage; a first NMOS transistor, connected to both ends of the first resistor, for short-circuiting the first resistor in response to a first program verify control signal and generating a program

verify voltage to a connecting point of a drain of the PMOS transistor, the first resistor, and its drain; a second NMOS transistor, connected to both ends of the second resistor, for short-circuiting the second resistor in response to a second program verify control signal; and a comparator for comparing a node voltage and a reference voltage between the first and second resistors, wherein an output of the comparator is connected to a gate of the PMOS transistor. The first and second program verify control signals are selectively activated to change the program verify voltage level. The wordline level selecting section applies a program voltage, a read voltage, a pass voltage or an erase voltage to wordlines of the flash memory cells according to operation modes.

In order to achieve the other object, the present invention provides a method for verifying whether one or more flash memory cells are programmed, the method including a first step to apply a predetermined program voltage to the flash memory cells; a second step to generate a program verify voltage in selective response to program verify control signals; and a third step to verify whether the flash memory cells are programmed, in response to the program verify voltage. A program unit loop cycle including the first to third steps is iteratively performed until the flash memory cells are completely programmed, and the program verify voltage is fluctuated at the respective program unit loop cycles.

Accordingly, a program verify operation is performed while changing a program verify voltage level to completely program flash memory cells having an uncertainty that they are programmed.

FIG. 4 shows a flash memory device according to an embodiment of the present invention. Referring to this figure, a flash memory device 400 is substantially identical to the flash memory device shown in FIG. 1 except that the flash memory device 400 further includes a program verify voltage generating section 410. The program verify generating section 410

includes a PMOS transistor 413 and first to third resistors 414, 415, and 416 serially coupled between a power supply voltage VCC and a ground voltage VSS, a first NMOS transistor connected to both ends of the first resistor 414, and a second NMOS transistor connected to both ends of the second resistor 415. A PMOS transistor 412 is gated to an output of a comparator 412 for comparing a reference voltage VREF and an NA node voltage between first to third resistors. The first NMOS transistor 417 is gated by a first program verify control signal PGM_VFEN1 to short-circuit the first resistor 414, and the second NMOS transistor 418 is gated to a second program verify control signal PGM_VFEN2 to short-circuit the second resistor 415.

The program verify voltage generating section 410 selectively short-circuits the first resistor 414 or the second resistor 415 depending on whether the first program verify control signal PGM_VFEN1 or the second program control signal PGM_VFEN2 is activated, so that a program verify voltage VRDV is generated high or low. If the first and second program verify control signals PGM_VFEN1 and PGM_VFEN2 are deactivated, the program verify voltage VRDV is generated high. If they are activated, the program verify voltage VRDV is generated low. Alternatively, if the they are selectively activated, the program verify voltage VRDV is generated to have various voltage levels.

FIG. 5 shows a first exemplary program verify method adopting a program verify voltage VRDV generated by a program verify voltage generating section 410. In an (n-2)th program unit loop, a program verify operation is performed using a first program verify voltage VRDV1 after performing a program operation using a first program voltage VPGM. In an (n-1)th program unit loop, a program verify operation is performed using a second program verify voltage higher VRDV2 than the first program verify voltage VRDV1 after performing a program operation using the second program voltage VPGM2. In an nth program unit loop, a program verify

operation is performed using the first program verify voltage VPGM1 higher than the second program verify voltage VPGM2. In an (n+1)th program unit loop, a program verify operation is performed using the second program verify voltage VRDV2 lower than the first program verify voltage VRDV1 after performing a program verify operation using a fourth program voltage VPGM4.

In each program unit loop, if a voltage having a level higher or lower than a previous program verify voltage VRDV is applied to perform a program verify operation, practically unprogrammed flash memory cells are determined to be programmed at a second program verify voltage VRDV2 and to be unprogrammed at a first program verify voltage VRDV1. Therefore, a program operation is re-performed to completely program the unprogrammed flash memory cells.

FIG. 6 shows distribution of flash memory cells based on the program verify method according to the present invention. Referring to this figure, in an initial state, a threshold voltage Vt of flash memory cells has a negative voltage level. While fluctuating a program verify voltage VRDV, a program unit loop is repeated to be uncertain whether flash memory cells having a threshold voltage Vt near a second program verify voltage VRDV2 are programmed, in an (n-1)th program unit loop. In an nth program unit loop, the flash memory cells having a lower threshold voltage Vt than the first program verify voltage VRDV1, i.e., flash memory cells that are uncertain whether they are programmed are determined to be unprogrammed and thus a program operation is re-performed. As a result, the threshold voltage Vt of the flash memory cells are uniformly distributed in the final program unit loop to erase under-program flash memory cells and over-program flash memory cells.

FIG. 7 is a second exemplary program verify timing diagram adopting a program verify voltage according to the present invention.

Referring to this figure, when program unit loops are sequentially performed, program verify operations are performed using program verify voltages VPGM1, VPGM2, VPGM3, and VPGM4 while the program verify voltages VPGM1, VPGM2, VPGM3, and VPGM4 rise at each loop. The first to fourth program verify voltages VPGM1, VPGM2, VPGM3, and VPGM4 have different voltage levels.

FIG. 8 is a third exemplary program verify timing diagram adopting a program verify voltage according to the present invention. Referring to this figure, the program verify voltage level in the nth program unit loop cycle is set to be higher than the program verify voltage level in the (n+1)th program unit loop cycle, and the program verify voltage level in the nth program unit loop cycle is set to be higher than the program verify voltage level in the (n+1)th program unit loop cycle. Unlike this, the program verify voltage level in the nth program unit loop cycle is set to be lower than the program verify voltage level in the (n-1)th program unit loop cycle, and the program verify voltage level in the (n+1)th program unit loop cycle is set to be lower than the program verify voltage level in the nth program unit loop cycle.

Although the present invention has been described with reference to the preferred embodiments thereof, it will be understood that the invention is not limited to the details thereof. Various substitutions and modifications have been suggested in the foregoing description, and other will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

[Effect of the Invention]

According to the present invention, a program verify operation is performed while changing a program verify voltage level to completely

program flash memory cells that are uncertain whether they are programmed.

[Scope of the Claim]

[Claim 1]

A flash memory device comprising:

a memory cell array block in which a plurality of flash memory cells are arranged;

a program verify voltage generating section for variably generating a program verify voltage for checking whether the flash memory cells are programmed; and

a wordline level selecting section for transferring the program verify voltage to a wordline connected to a control gate of the flash memory cells.

[Claim 2]

The flash memory device of Claim 1, wherein the program verify voltage generating section comprises:

a PMOS transistor and first to third resistors serially coupled between a power supply voltage and a ground voltage;

a first NMOS transistor, connected to both ends of the first resistor, for short-circuiting the first resistor in response to a first program verify control signal and generating a program verify voltage to a connecting point of a drain of the PMOS transistor, the first resistor, and its drain;

a second NMOS transistor, connected to both ends of the second resistor, for short-circuiting the second resistor in response to a second program verify control signal; and

a comparator for comparing a node voltage and a reference voltage between the first and second resistors, wherein an output of the comparator is connected to a gate of the PMOS transistor.

[Claim 3]

The flash memory device of Claim 2, wherein the first and second program verify control signals are selectively activated to change the program verify voltage level.

[Claim 4]

The flash memory device of Claim 1, wherein the wordline level selecting section applies a program voltage, a read voltage, a pass voltage or an erase voltage to wordlines of the flash memory cells according to operation modes.

[Claim 5]

A method for verifying whether one or more flash memory cells are programmed, the method comprising:

a first step to apply a predetermined program voltage to the flash memory cells;

a second step to generate a program verify voltage in selective response to program verify control signals; and

a third step to verify whether the flash memory cells are programmed, in response to the program verify voltage,

wherein a program unit loop cycle including the first to third steps is iteratively performed until the flash memory cells are completely programmed, and the program verify voltage is fluctuated at the respective program unit loop cycles.

[Claim 6]

The method of Claim 5, wherein the program verify voltage level in the nth program unit loop cycle is higher than the program verify voltage level in the (n-1)th, and the program verify voltage level in the (n+1)th

program unit loop cycle is higher than the program verify voltage level in the nth program unit loop cycle.

[Claim 7]

The method of Claim 6, wherein the program verify voltage level in the (n-1)th program unit loop cycle is identical to the program verify voltage level in the (n+1)th program unit loop cycle.

[Claim 8]

The method of Claim 6, wherein the program verify voltage level in the (n-1)th program unit loop cycle, the program verify voltage level in the nth program unit loop cycle, and the (n+1)th program unit loop cycle are different from each other.

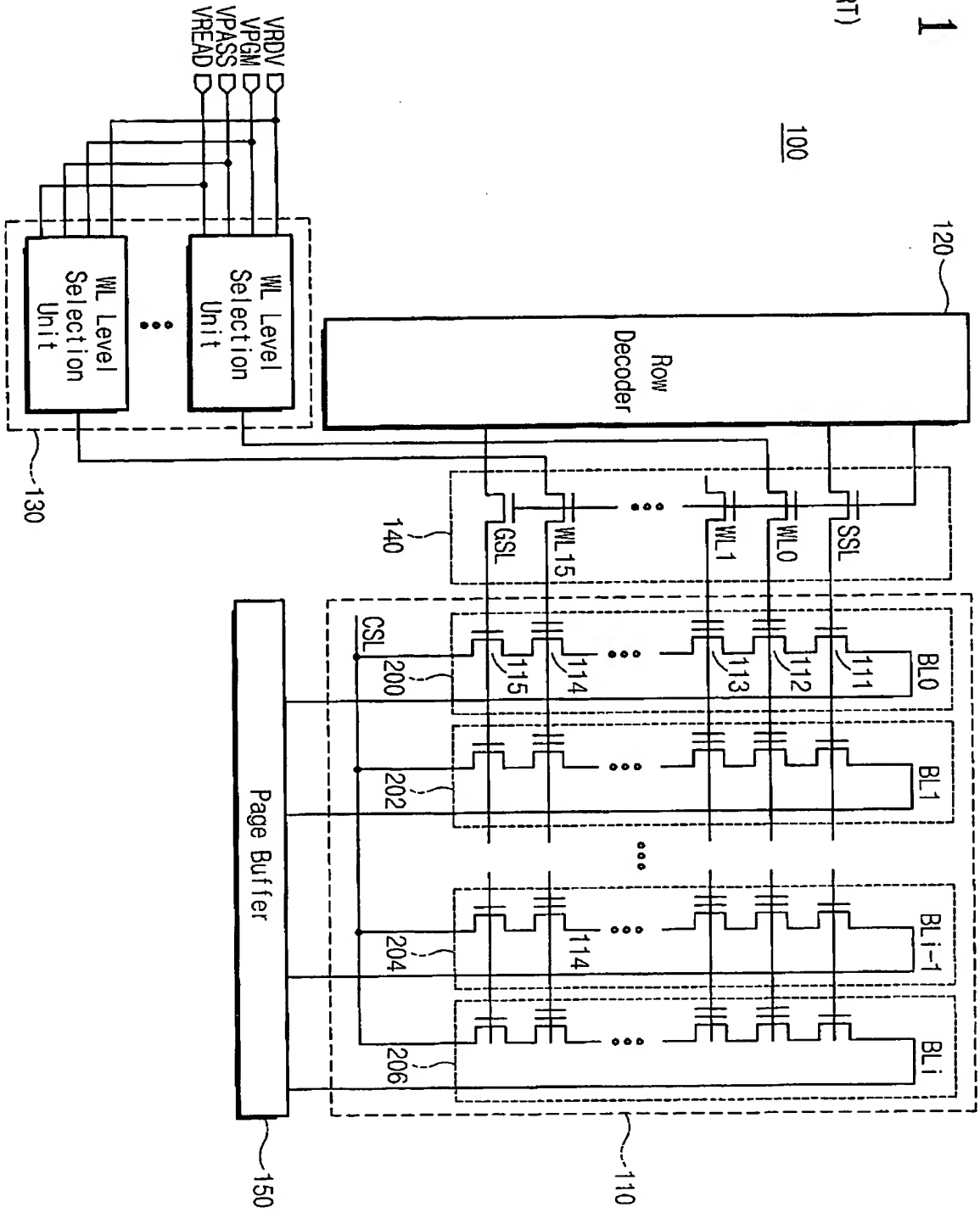
[Claim 9]

The method of Claim 5, wherein the program verify voltage level in the nth program unit loop cycle is set to be higher than the program verify voltage level in the (n+1)th program unit loop cycle, and the program verify voltage level in the nth program unit loop cycle is set to be higher than the program verify voltage level in the (n+1)th program unit loop cycle.

[Claim 10]

The method of Claim 5, wherein the program verify voltage level in the nth program unit loop cycle is set to be lower than the program verify voltage level in the (n-1)th program unit loop cycle, and the program verify voltage level in the (n+1)th program unit loop cycle is set to be lower than the program verify voltage level in the nth program unit loop cycle.

Fig. 1
(PRIOR ART)



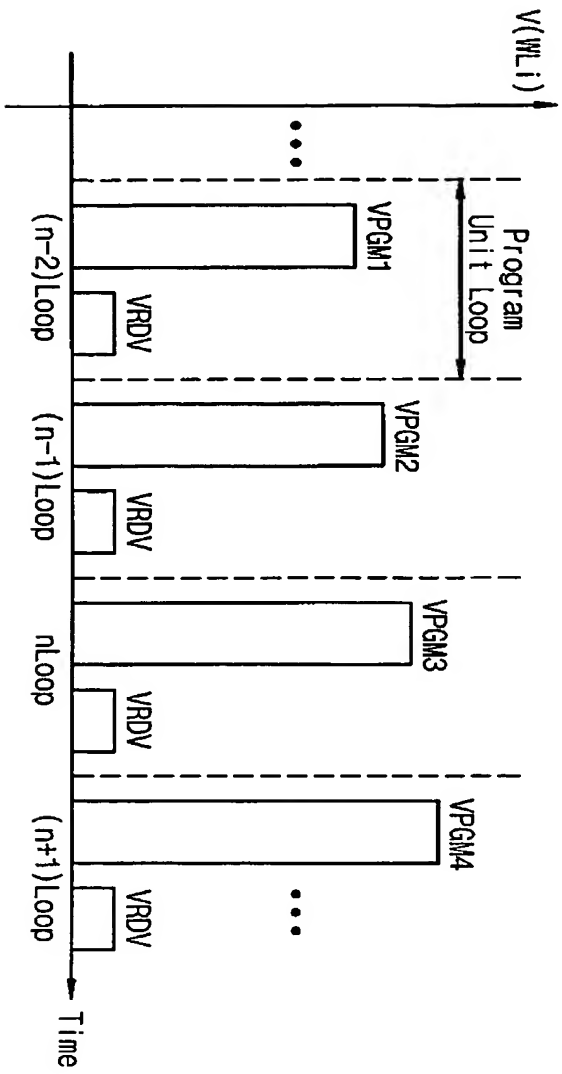
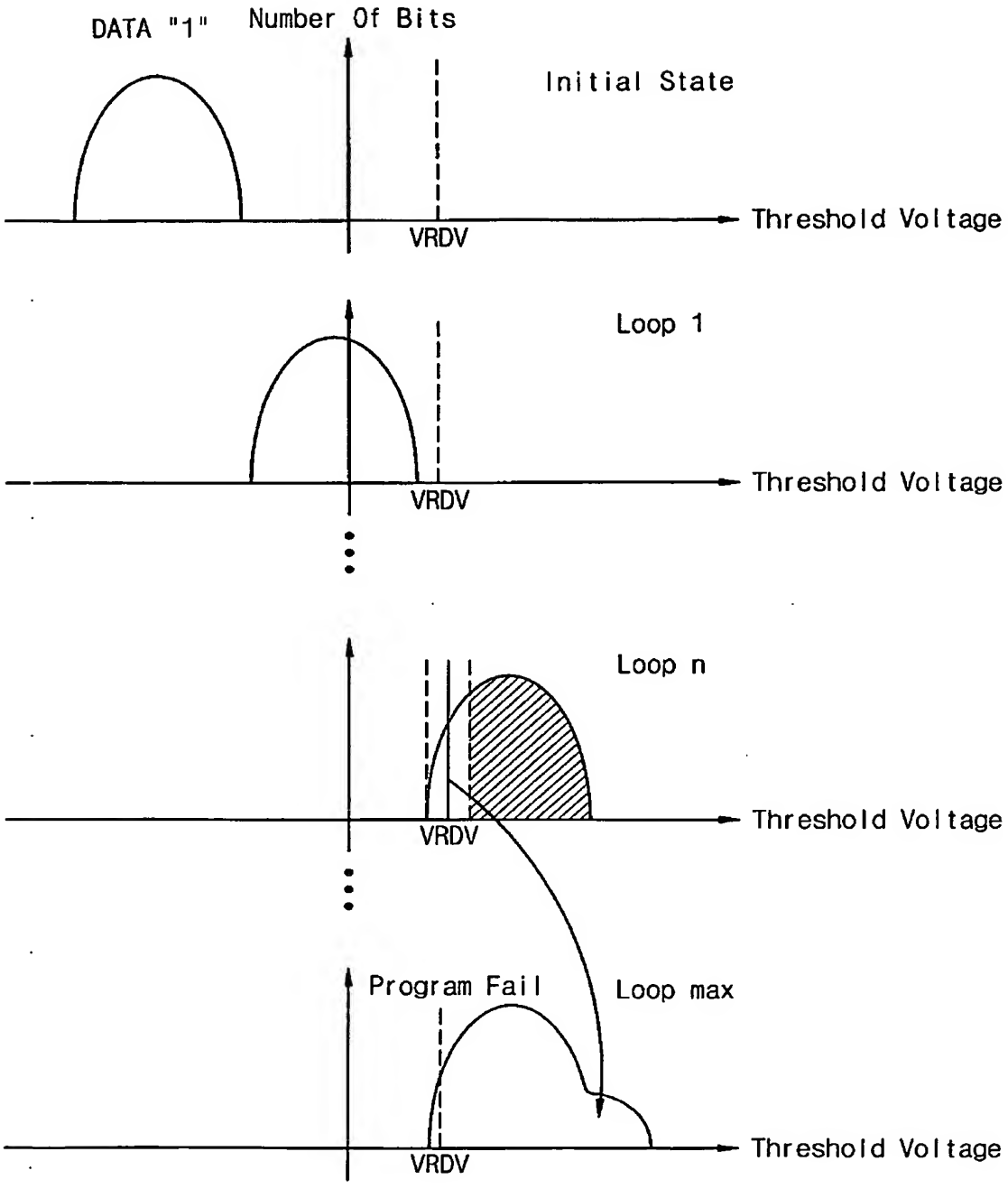
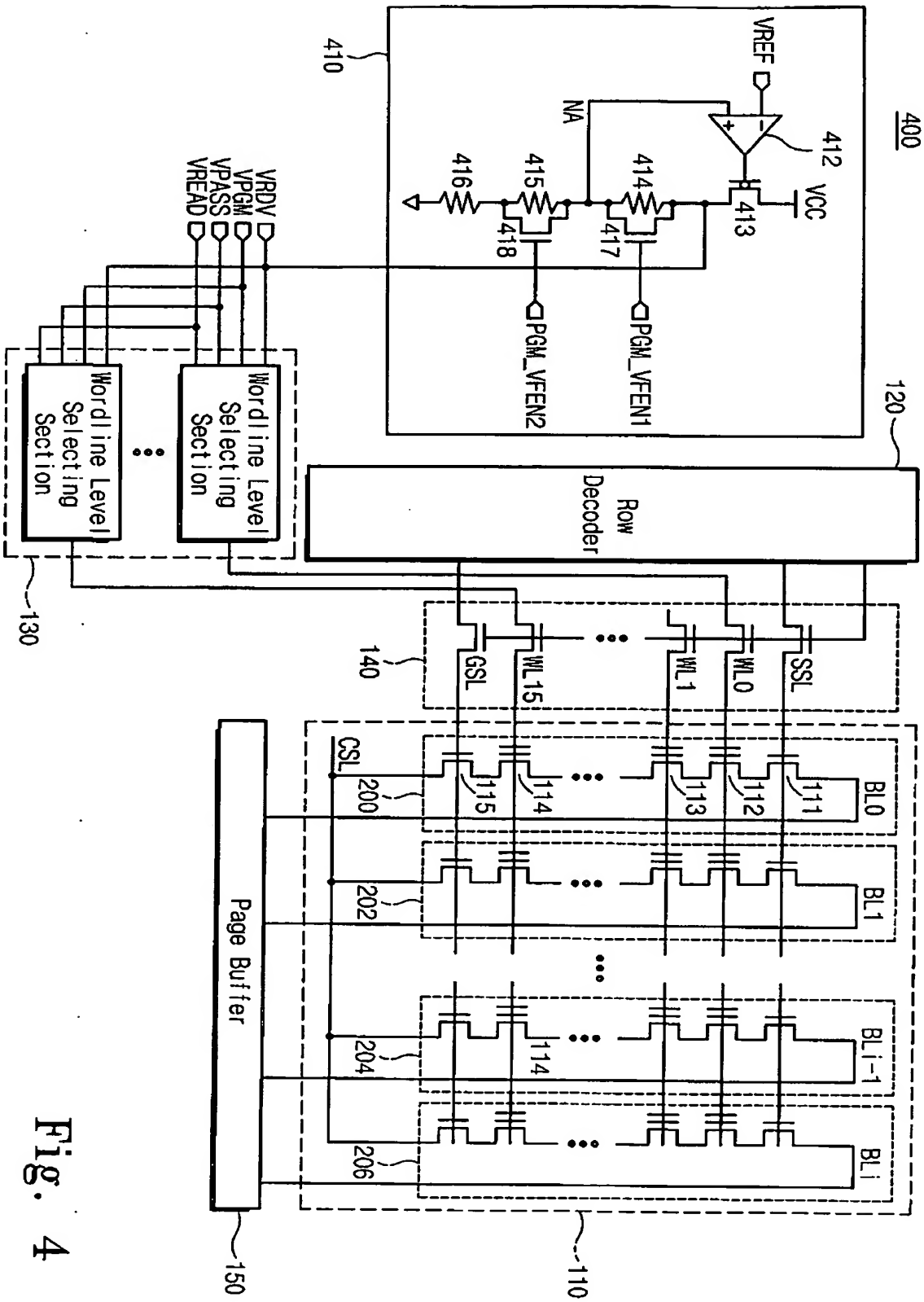

V(WLi)
Program Unit Loop
VPGM1
VRDV
VPGM2
VRDV
VPGM3
VRDV
VPGM4
VRDV
(n-2)Loop
(n-1)Loop
nLoop
(n+1)Loop
Time

Fig. 2

Fig. 3


DATA "1"
Number Of Bits
Initial State
Threshold Voltage
VRDV
Loop 1
Threshold Voltage
VRDV
Loop n
Threshold Voltage
VRDV
Program Fail
Loop max
Threshold Voltage
VRDV


400
410
VREF
NA
412
VCC
413
414
415
416
417
418
PGM_VFEN1
PGM_VFEN2
VRDV
VPGM
VPASS
VREAD
120
Row Decoder
Wordline Level Selecting Section
Wordline Level Selecting Section
130
140
GSL
WL15
WL1
WL0
SSL
CSL
200
202
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111
112
113
114
115
BL0
BL1
BLi-1
BLi
Page Buffer
150
110

Fig. 4

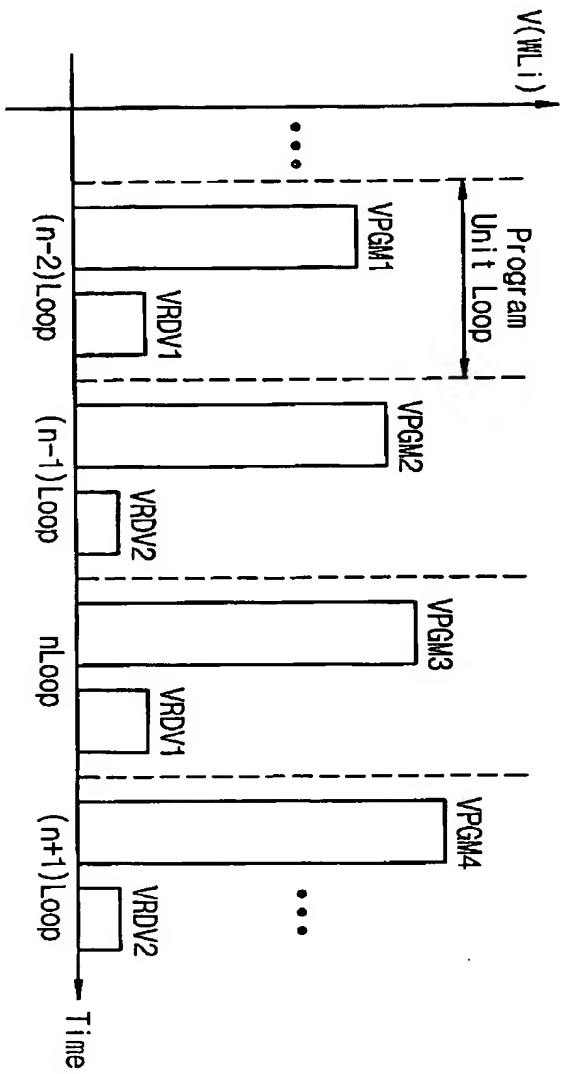
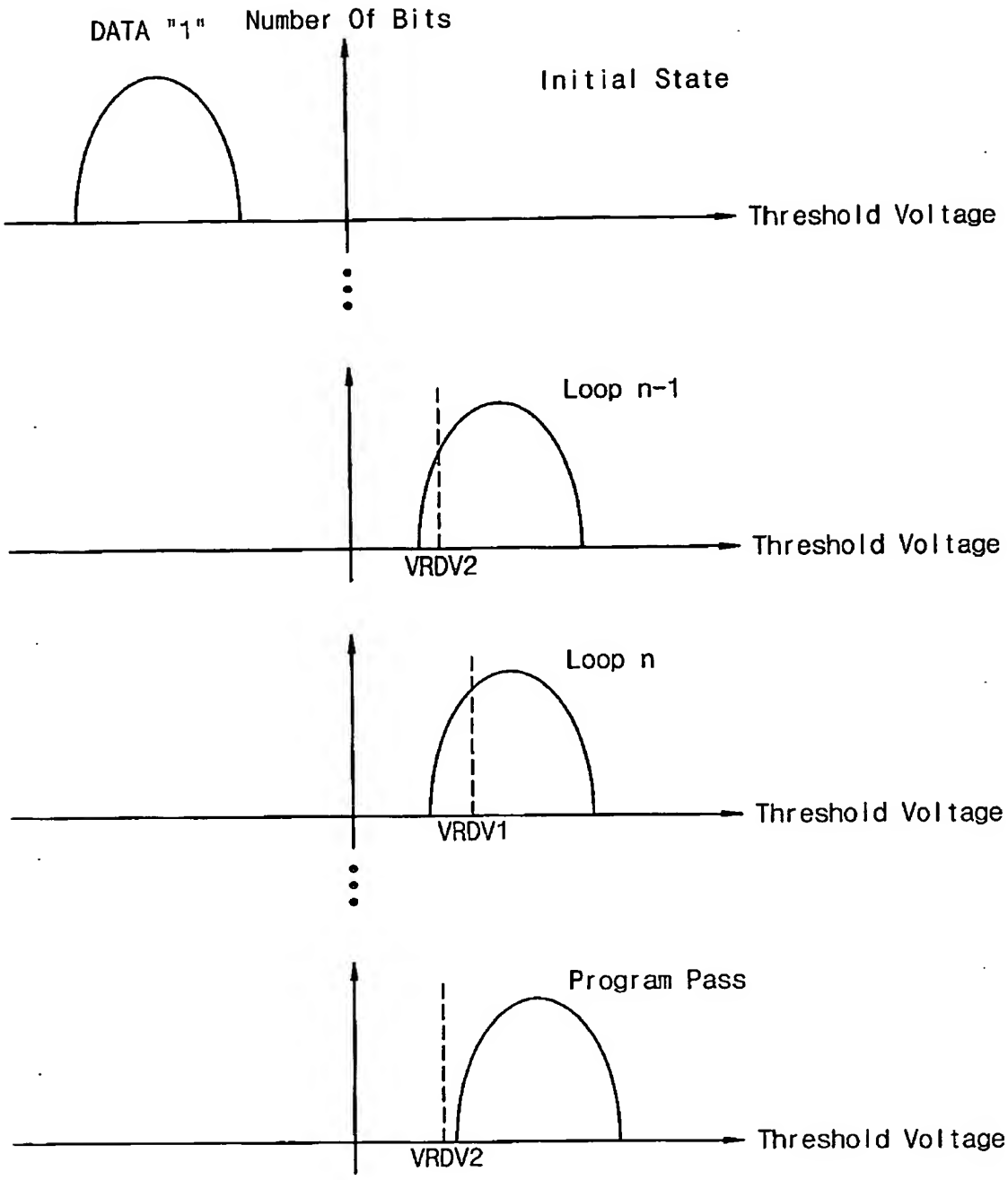

V(WLi)
Program
Unit Loop
VPGM1
VRDV1
VPGM2
VRDV2
VPGM3
VRDV1
VPGM4
VRDV2
(n-2)Loop
(n-1)Loop
nLoop
(n+1)Loop
Time

Fig. 5

Fig. 6


DATA "1"
Number Of Bits
Initial State
Threshold Voltage
Loop n-1
VRDV2
Threshold Voltage
Loop n
VRDV1
Threshold Voltage
Program Pass
VRDV2
Threshold Voltage

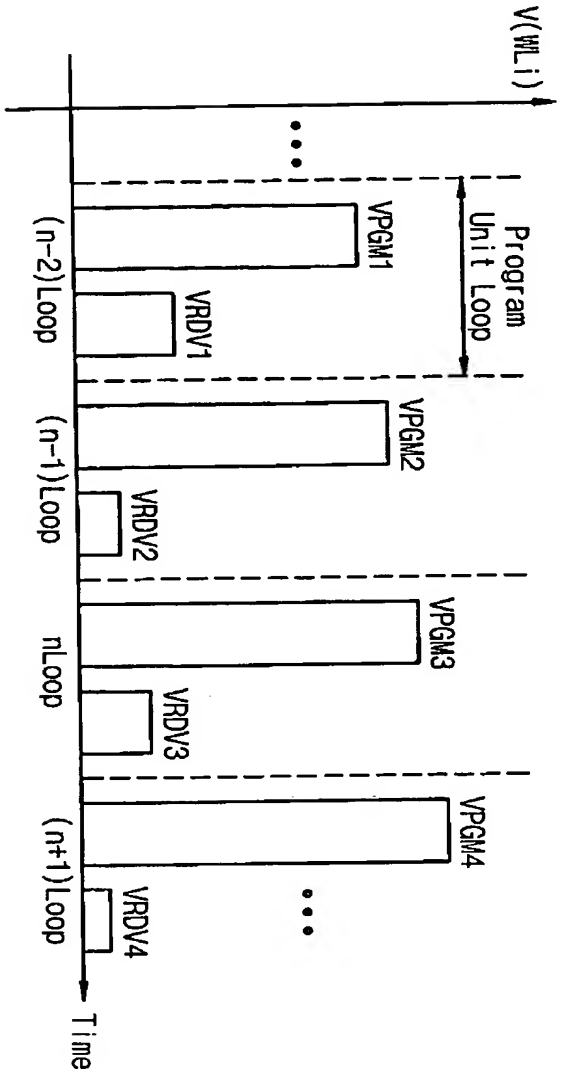

V(WLi)
Program
Unit Loop
VPGM1
VRDV1
VPGM2
VRDV2
VPGM3
VRDV3
VPGM4
VRDV4
(n-2)Loop
(n-1)Loop
nLoop
(n+1)Loop
Time

Fig. 7

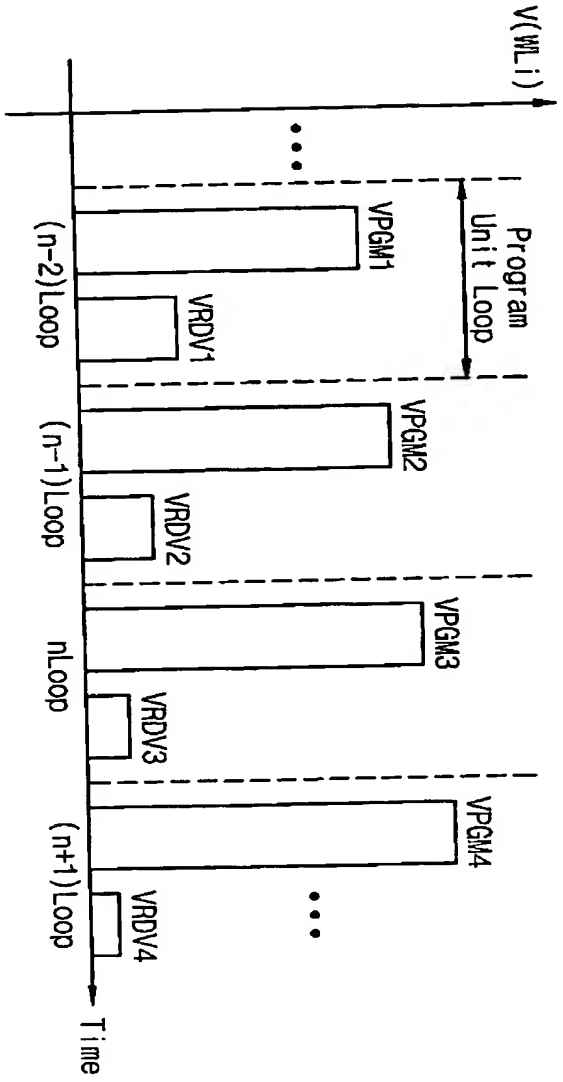

V(WLi)
Program
Unit Loop
VPGM1
VRDV1
(n-2)Loop
VPGM2
VRDV2
(n-1)Loop
VPGM3
VRDV3
nLoop
VPGM4
VRDV4
(n+1)Loop
Time

Fig. 8